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EXAMINER	
MASON, DONNA K	

ART UNIT	PAPER NUMBER
2111	5

DATE MAILED: 02/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/896,769	Applicant(s) ABRAMSON ET AL.	
	Examiner Donna K. Mason	Art Unit 2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 June 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,755,939 to Watson.

With regard to claim 1, Watson discloses a method including removing a work item from an enabled bus schedule data structure and generating a coherency signal in response to removing the work item (column 2, lines 44-46), and reclaiming the work item in response to generating the coherency signal (column 2, lines 47-48).

Therefore, Watson reads on the invention as claimed.

4. Claims 1 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,502,111 to Dussud.

With regard to claims 1 and 11, Dussud discloses a method including removing a work item from an enabled bus schedule data structure and generating a coherency signal in response to removing the work item (column 9, lines 7-9), and reclaiming the work item in response to generating the coherency signal (column 9, lines 3-7).

Also, with regard to claim 11, Dussud discloses a machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform the claimed method (Fig. 2, items 120, 124, and 106).

Therefore, Dussud reads on the invention as claimed.

5. Claims 21, 22, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by *Universal Host Controller Interface (UHCI) Design Guide*, Rev. 1.1, by Intel ("Intel").

With regard to claims 21 and 27, Intel discloses an apparatus and computer system including a command register having a command bit (pages 11-12, section 2.1.1), a status register having a status bit (pages 13-14, section 2.1.2), and a microcontroller to process the data expansion bus schedule data structure (page 6, section 1.2.3) and to modify the status signal bit in response to the removal of the work item (pages 13-14, section 2.1.2).

With regard to claim 22, Intel discloses the apparatus where the expansion bus schedule data structure includes a Universal Serial Bus (USB) asynchronous schedule (page 7, section 1.3).

Therefore, Intel reads on the invention as claimed.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watson in view of Intel.

As described above with regard to the 35 U.S.C. 102(b) rejection of claim 1, Watson discloses all the features of claim 1. Watson does not expressly disclose all the features of dependent claims 2-4 and 10.

With regard to claims 2-4, Intel discloses the method where the enabled expansion bus schedule data includes an asynchronous schedule including a plurality of queue heads, and removing the work item includes unlinking a first queue head (page 7, section 1.3). Intel also discloses a second queue head, which includes a horizontal link pointer to the first queue head (page 31, section 3.4.2). Furthermore, Intel discloses the step of generating a command signal in response to removing the work item (pages 11-12, section 2.1.1), and where the step of generating a coherency signal includes the step of generating a status signal (page 13-14, section 2.1.2).

With regard to claim 10, Intel discloses the method further including storing each of the work items in a memory, where reclaiming the work item includes freeing a portion of memory associated with the work item (page 7, section 1.3).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Intel with the apparatus of Watson. The suggestion or motivation for doing so would have been to increase system performance, reduce hardware complexity, and to minimize costs (*see* pages 1-2 of Intel).

Therefore, it would have been obvious to combine Intel with Watson to obtain the invention as specified in claims 2-4 and 10.

8. Claims 2-5, 10, 12-15, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dussud in view of Intel.

As described above with regard to the 35 U.S.C. 102(e) rejection of claims 1 and 11, Dussud discloses all the features of claims 1 and 11. Dussud does not expressly disclose all the features of dependent claims 2-5, 10, 12-15, and 20.

With regard to claims 2-4, Intel discloses the method where the enabled expansion bus schedule data includes an asynchronous schedule including a plurality of queue heads, and removing the work item includes unlinking a first queue head (page 7, section 1.3). Intel also discloses a second queue head, which includes a horizontal link pointer to the first queue head (page 31, section 3.4.2). Furthermore, Intel discloses the step of generating a command signal in response to removing the work item (pages 11-12, section 2.1.1), and where the step of generating a coherency signal includes the step of generating a status signal (page 13-14, section 2.1.2).

With regard to claims 5 and 15, Dussud discloses the method where generating a coherency signal includes the steps of storing a copy of a work item within a memory and generating a coherency signal using a copy of the work item (column 2, lines 10-20). Dussud does not disclose the step of traversing the work items according to a sequnce. Intel discloses this feature, as described on page 6, section 1.2.3.

With regard to claims 10 and 20, Intel discloses the method further including storing each of the work items in a memory, where reclaiming the work item includes freeing a portion of memory associated with the work item (page 7, section 1.3).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Intel with the apparatus of Dussud. The suggestion or motivation for doing so would have been to increase system performance, reduce hardware complexity, and to minimize costs (*see* pages 1-2 of Intel).

Therefore, it would have been obvious to combine Intel with Dussud to obtain the invention as specified in claims 2-5, 10, 12-15, and 20.

9. Claims 6-9 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dussud in view of Intel as applied to claims 5 and 15 above, and further in view of U.S. Patent No. 6,128,654 to Runaldue, et al. ("Runaldue").

As described with regard to the 35 U.S.C. 103(a) rejection above, Dussud in view of Intel discloses all the features of claims 5 and 15. Dussud in view of Intel does not expressly disclose all the features of claims 6-9 and 16-19.

Runaldue discloses the method, where generating a coherency signal using the copy of the work item includes detecting a removal of the copy of the work item, and

generating a coherency signal in response to removing the copy. Runaldue also discloses the method where detecting a removal of copy of the work item includes detecting a cache flush operation, where generating a coherency signal includes identifying an accessible work item and generating a coherency signal, and the method further including executing a transaction on a USB (*see* column 13, lines 15-66).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Runaldue with Dussud in view of Intel. The suggestion or motivation for doing so would have been to transmit multiple copies of a set of data, using a reduced amount of memory space in the transmitting device and in the memory overall (column 1, lines 54-57).

Therefore, it would have been obvious to combine Runaldue with Dussud and Intel to obtain the invention as specified in claims 6-9 and 16-19.

10. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watson in view of U.S. Patent Application Publication No. 2002/0133533 to Czajkowski, et al. ("Czajkowski").

With regard to claim 11, Watson discloses the steps of removing a work item from an enabled bus schedule data structure and generating a coherency signal in response to removing the work item (column 2, lines 44-46), and reclaiming the work item in response to generating the coherency signal (column 2, lines 47-48).

Watson does not expressly disclose a machine-readable medium that provides instructions, which when executed by a machine, cause the machine to perform the

disclosed steps. Czajkowski discloses a machine-readable medium, as described in paragraph [0033].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the machine-readable medium of Czajkowski with the steps of Watson. The suggestion or motivation for doing so would have been to provide a storage medium for the instructions.

Therefore, it would have been obvious to combine Czajkowski with Watson to obtain the invention as specified in claim 11.

11. Claims 12-14 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watson in view of Czajkowski as applied to claim 1 above, and further in view of Intel.

As described above with regard to the 35 U.S.C. 103(a) rejection of claim 11, Watson in view of Czajkowski discloses all the features of claim 11. Watson in view of Czajkowski does not expressly disclose all the features of dependent claims 12-14 and 20.

With regard to claims 12-14, Intel discloses the method where the enabled expansion bus schedule data includes an asynchronous schedule including a plurality of queue heads, and removing the work item includes unlinking a first queue head (page 7, section 1.3). Intel also discloses a second queue head, which includes a horizontal link pointer to the first queue head (page 31, section 3.4.2). Furthermore, Intel discloses the step of generating a command signal in response to removing the work

item (pages 11-12, section 2.1.1), and where the step of generating a coherency signal includes the step of generating a status signal (page 13-14, section 2.1.2).

With regard to claim 20, Intel discloses the method further including storing each of the work items in a memory, where reclaiming the work item includes freeing a portion of memory associated with the work item (page 7, section 1.3).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Intel with the apparatus of Watson in view of Czajkowski. The suggestion or motivation for doing so would have been to increase system performance, reduce hardware complexity, and to minimize costs (*see* pages 1-2 of Intel).

Therefore, it would have been obvious to combine Intel with Watson in view of Czajkowski to obtain the invention as specified in claims 12-14 and 20.

12. Claims 23-26 and 28-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel in view of Runaldue.

As described with regard to the 35 U.S.C. 102(a) rejection above, Intel discloses all the features of claims 21 and 27. Intel does not expressly disclose all the features of claims 23-26 and 28-30.

Runaldue discloses the apparatus and computer system including a cache memory to store a copy of a work item, a microcontroller to modify the status signal bit, where the microcontroller modifies the status signal bit in response to a cache flush operation, and where the microcontroller identifies an accessible work item (*see* column 13, lines 15-66).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine Runaldue with Intel. The suggestion or motivation for doing so would have been to transmit multiple copies of a set of data, using a reduced amount of memory space in the transmitting device and in the memory overall (column 1, lines 54-57).

Therefore, it would have been obvious to combine Runaldue with Intel to obtain the invention as specified in claims 23-26 and 28-30.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donna K. Mason whose telephone number is (703) 305-1887. The examiner can normally be reached on Monday - Friday, 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on (703) 305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

XUAN M. THAI
PRIMARY EXAMINER
TC2100

DKM